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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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KNOBBE MARTENS OLSON & BEAR LLP
2040 MAIN STREET
FOURTEENTH FLOOR
IRVINE, CA 92614

EXAMINER

WILKINS III, HARRY D

ART UNIT	PAPER NUMBER
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1742

DATE MAILED: 05/15/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/705,360

Applicant(s)

BASOL, BULENT M.

Examiner

Harry D. Wilkins, III

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☐ Responsive to communication(s) filed on ____.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-18 is/are pending in the application.
- 4a) Of the above claim(s) ____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) ____ is/are allowed.
- 6) ☒ Claim(s) 1-18 is/are rejected.
- 7) ☒ Claim(s) 10 is/are objected to.
- 8) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 10 November 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. ____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. ____. |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date <u>5/4/04</u> . | 6) <input type="checkbox"/> Other: ____. |

DETAILED ACTION

Claim Objections

1. Claim 10 is objected to because of the following informalities: "planer" should be "planar". Appropriate correction is required.

Claim Interpretation

2. The claim term "low temperature processing environment", has been sufficiently described in the specification, such that one of ordinary skill in the art would understand that the claimed method operates at temperatures below ambient, but above the freezing point of the liquid electrolyte. As such, this claim term has been limited by the specification to exclude temperatures outside this range.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 1, 4-6, 8-15, 17 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Creutz et al (US 4,110,176) in view of Andricacos et al (US 5,516,412) and Rodbell et al (US 6,344,129).

Creutz et al teach (see abstract and cols. 3 and 4) electroplating copper on a substrate having a conductive surface including wetting the conductive surface with an electrolyte solution having a brightening agent. The brightening agent becomes

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adsorbed onto the entire conductive surface to facilitate electroplating. The process further included processing of the conductive surface by electroplating.

Thus, Creutz et al fail to teach (1) electroplating on a substrate that included a conductive surface with a top portion and a cavity portion, (2) applying an external influence to the top portion, the influence removing a part of the brightener adsorbed on the top portion and (3) maintaining a low temperature environment.

Andricacos et al teach (see abstract, figures 1-4 and associated description) the concept of electroplating on a microelectronic substrate that included top portions and cavity portions and applying an external influence through sweeping element 28.

Rodbell et al teach (see abstract and paragraph spanning cols. 5 and 6) performing electroplating of copper on a microelectronic substrate that included top portions and cavity portions at reduced temperatures (0-18°C) for the purpose of decreasing the dopant levels in the electroplated copper layer.

Therefore, it would have been obvious to one of ordinary skill in the art (1) to have applied the electroplating method of Creutz et al to a substrate that included a conductive surface that included both a top portion and a cavity portion because Andricacos et al and Rodbell et al teach the desirability of using copper electroplating to make microelectronic devices; (2) to have used the device/method of Andricacos et al to have applied an external influence using the sweeping element 28 to the substrate because Andricacos et al teach (see col. 9, lines 49-53) that the sweeping element was able to provide effective agitation of the electrolyte and fluid flow patterns that were accurately reproducible for repetitive, high-volume uses; and, (3) to have maintained the

electroplating environment at a low temperature as suggested by Rodbell et al for the purpose of decreasing dopant levels in the electroplated copper layer.

With respect to the limitation "the external influence removing a part of the first amount of the additive adsorbed on the top portion", the sweeping element of Andricacos et al would have been expected to have performed this function since it agitated the electrolyte in the vicinity of the conductive surface. If Applicant disagrees with this assessment, comparative results should be submitted which show that the sweeping process of Andricacos et al did not produce the claimed "removing".

Regarding claim 4, Rodbell et al fail to teach or suggest how the lowered temperature processing environment was achieved. However, Andricacos et al teach (see col. 6, lines 43-45) that suitable temperature control of the electrolyte was typically provided. Thus, it would have been obvious to one of ordinary skill in the art to have provided the low temperature of Rodbell et al by cooling the electrolyte solution.

Regarding claim 5, Rodbell et al suggest temperatures of 0-18°C, preferably 5-15°C and most preferably 8-12°C.

Regarding claim 6, Andricacos et al suggest using a sweeper to applying the external influence with the sweeper.

Regarding claim 8, although Creutz et al teach electroplating of copper, Andricacos et al teach (see col. 9, lines 43-47) that electroetching of copper was known to be performed in a similar fashion by reversing the polarity of the electrodes. Therefore, it would have been obvious to have performed electroetching when removal of copper was necessary.

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Regarding claim 9, the processing of Creutz et al was electroplating.

Regarding claim 10, Rodbell et al teach forming a first layer by electroplating using a first electrolyte, and then forming a second layer by electroplating using a second electrolyte, wherein the first electroplating was used to fill holes and vias and the second electroplating was used to provide a planar overburden layer.

Regarding claim 11, Creutz et al and Andricacos et al teach wetting the conductive surface with an electrolyte solution having an additive adsorbed onto the conductive surface, applying an external influence by sweeping element 28, processing (electroplating) the conductive surface. Rodbell et al teach performing a two-phase electroplating process, wherein the second phase of the process was performed at a lower temperature than the first phase. Thus, Rodbell et al suggest an intermediate chilling step. The external influence and processing (electroplating) would have been reapplied after the lower temperature electrolyte was introduced to perform the second phase of the process.

Regarding claim 12, it would have been obvious to one of ordinary skill in the art to have utilized two distinct electrolyte solutions for the two-phase electroplating taught by Rodbell et al because of the different chemistry of reaction at the different processing temperatures.

Regarding claim 13, it would have been within the expected skill of a routineer in the art to have optimized the additive concentration in the first and second electrolytes to have adapted each solution to the specific conditions of the different phases.

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Regarding claim 14, Rodbell et al suggest temperatures of 0-18°C, preferably 5-15°C and most preferably 8-12°C.

Regarding claim 15, Andricacos et al teach a sweeper and sweeping the conductive surface with the sweeper.

Regarding claim 17, although Creutz et al teach electroplating of copper, Andricacos et al teach (see col. 9, lines 43-47) that electroetching of copper was known to be performed in a similar fashion by reversing the polarity of the electrodes. Therefore, it would have been obvious to have performed electroetching when removal of copper was necessary.

Regarding claim 18, the processing of Creutz et al was electroplating.

5. Claims 2 and 3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Creutz et al (US 4,110,176) in view of Andricacos et al (US 5,516,412) and Rodbell et al (US 6,344,129) as applied to claim 1 above, and further in view of Carl et al (US 6,436,267).

The teachings of Creutz et al, Andricacos et al and Rodbell et al are described above.

However, Rodbell et al was silent with respect to how to achieve the low temperature processing environment.

Carl et al teach (see paragraph spanning cols. 6 and 7) a method whereby the temperature of a semiconductor substrate to be processed is chilled by first chilling the substrate support and contacting the wafer with the chilled support.

Therefore, it would have been obvious to one of ordinary skill in the art to have performed the step of maintaining a low temperature processing environment of Rodbell et al by cooling the substrate support and contacting the wafer with the substrate support.

With respect to the fact that the substrate support of Carl et al was used for PVD deposition of a seed layer and not electroplating, one of ordinary skill in the art would have realized that the substrate support of Carl et al with cooling fluid channels, could have been used with any semiconductor substrate process, such as electroplating, where such temperature control was necessary.

6. Claims 1 and 4-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Creutz et al (US 4,110,176) in view of Uzoh et al (US 6,354,916) and Rodbell et al (US 6,344,129).

Creutz et al teach (see abstract and cols. 3 and 4) electroplating copper on a substrate having a conductive surface including wetting the conductive surface with an electrolyte solution having a brightening agent. The brightening agent becomes adsorbed onto the entire conductive surface to facilitate electroplating. The process further included processing of the conductive surface by electroplating.

Thus, Creutz et al fail to teach (1) electroplating on a substrate that included a conductive surface with a top portion and a cavity portion, (2) applying an external influence to the top portion, the influence removing a part of the brightener adsorbed on the top portion and (3) maintaining a low temperature environment.

Uzoh et al teach (see abstract, figure 2 and associated description) the concept of electroplating on a microelectronic substrate that included top portions and cavity portions and applying an external influence through a polishing pad 8.

Rodbell et al teach (see abstract and paragraph spanning cols. 5 and 6) performing electroplating of copper on a microelectronic substrate that included top portions and cavity portions at reduced temperatures (0-18°C) for the purpose of decreasing the dopant levels in the electroplated copper layer.

Therefore, it would have been obvious to one of ordinary skill in the art (1) to have applied the electroplating method of Creutz et al to a substrate that included a conductive surface that included both a top portion and a cavity portion because Uzoh et al and Rodbell et al teach the desirability of using copper electroplating to make microelectronic devices; (2) to have used the device/method of Uzoh et al to have applied an external influence using the polishing pad 8 to the substrate because Uzoh et al teach (see col. 6, lines 7-55) that the polishing pad was able to provide effective planarization of the electroplated layer; and, (3) to have maintained the electroplating environment at a low temperature as suggested by Rodbell et al for the purpose of decreasing dopant levels in the electroplated copper layer.

With respect to the limitation "the external influence removing a part of the first amount of the additive adsorbed on the top portion", the polishing pad of Uzoh et al would have been expected to have performed this function since it disturbed to the top portion of the conductive surface. If Applicant disagrees with this assessment,

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comparative results should be submitted which show that the polishing process of Uzoh et al did not produce the claimed "removing".

Regarding claim 4, Rodbell et al fail to teach or suggest how the lowered temperature processing environment was achieved. However, it would have been obvious to one of ordinary skill in the art to have provided the low temperature of Rodbell et al by cooling the electrolyte solution since cooling of a liquid was a known method of providing a desired low temperature.

Regarding claim 5, Rodbell et al suggest temperatures of 0-18°C, preferably 5-15°C and most preferably 8-12°C.

Regarding claims 6 and 7, Uzoh et al suggest using a polishing pad to apply the external influence and the polishing pad contacted the top portions of the conductive surface.

Regarding claim 8, although Creutz et al teach electroplating of copper, Uzoh et al teach that material was removed from the surface of the conductive surface by action of the polishing pad.

Regarding claim 9, the processing of Creutz et al and Uzoh et al was electroplating/electrodeposition.

Regarding claim 10, Rodbell et al teach forming a first layer by electroplating using a first electrolyte, and then forming a second layer by electroplating using a second electrolyte, wherein the first electroplating was used to fill holes and vias and the second electroplating was used to provide a planar overburden layer.

Regarding claim 11, Creutz et al and Uzoh et al teach wetting the conductive surface with an electrolyte solution having an additive adsorbed onto the conductive surface, applying an external influence by polishing pad 8, processing (electroplating) the conductive surface. Rodbell et al teach performing a two-phase electroplating process, wherein the second phase of the process was performed at a lower temperature than the first phase. Thus, Rodbell et al suggest an intermediate chilling step. The external influence and processing (electroplating) would have been reapplied after the lower temperature electrolyte was introduced to perform the second phase of the process.

Regarding claim 12, it would have been obvious to one of ordinary skill in the art to have utilized two distinct electrolyte solutions for the two-phase electroplating taught by Rodbell et al because of the different chemistry of reaction at the different processing temperatures.

Regarding claim 13, it would have been within the expected skill of a routineer in the art to have optimized the additive concentration in the first and second electrolytes to have adapted each solution to the specific conditions of the different phases.

Regarding claim 14, Rodbell et al suggest temperatures of 0-18°C, preferably 5-15°C and most preferably 8-12°C.

Regarding claims 15 and 16, Uzoh et al teach a polishing pad and contacting the conductive surface with the pad.

Regarding claim 17, although Creutz et al teach electroplating of copper, Uzoh et al teach that material was removed from the surface of the conductive surface by action of the polishing pad.

Regarding claim 18, the processing of Creutz et al was electroplating.

7. Claims 2 and 3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Creutz et al (US 4,110,176) in view of Uzoh et al (US 6,354,916) and Rodbell et al (US 6,344,129) as applied to claim 1 above, and further in view of Carl et al (US 6,436,267).

The teachings of Creutz et al, Uzoh et al and Rodbell et al are described above.

However, Rodbell et al was silent with respect to how to achieve the low temperature processing environment.

Carl et al teach (see paragraph spanning cols. 6 and 7) a method whereby the temperature of a semiconductor substrate to be processed is chilled by first chilling the substrate support and contacting the wafer with the chilled support.

Therefore, it would have been obvious to one of ordinary skill in the art to have performed the step of maintaining a low temperature processing environment of Rodbell et al by cooling the substrate support and contacting the wafer with the substrate support.

With respect to the fact that the substrate support of Carl et al was used for PVD deposition of a seed layer and not electroplating, one of ordinary skill in the art would have realized that the substrate support of Carl et al with cooling fluid channels, could have been used with any semiconductor substrate process, such as electroplating, where such temperature control was necessary.

Double Patenting

8. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

9. Claims 1-18 are rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-30 of U.S. Patent No. 6,534,116 in view of Rodbell et al (US 6,344,129). The claims of 6,534,116 teach the invention as claimed, with the exception of the requirement that the processing environment be kept at a low temperature. However, such feature would have been obvious to one of ordinary skill in the art in view of the teachings of Rodbell et al regarding the fact that a low temperature environment allowed a more pure electroplated copper layer to be formed. The various features of other dependent claims would also have been obvious to one of ordinary skill in the art similarly as described in the rejection grounds above.

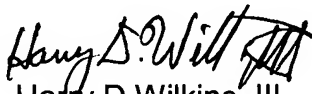
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Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Harry D. Wilkins, III whose telephone number is 571-272-1251. The examiner can normally be reached on M-F 8:30am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Roy V. King can be reached on 571-272-1244. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).


Harry D Wilkins, III
Primary Examiner
Art Unit 1742

hdw